REMARKS

The indication of allowable subject matter in claims 3 and 14 is acknowledged and appreciated. Further, it is noted that there is no pending rejection against claims 15-16 (added in the amendment filed with an RCE on December 27, 2004). Therefore, we believe that claims 15-16 would be patentable. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 1-16 are objected for using a "/" because it is allegedly unclear whether "/" is considered "or" or "and." In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Koyama to discuss this issue. During the interview, it was agreed that the claims could maintain the use of "/" and would mean "and/or" ("and/or" not recited in claims merely to avoid unnecessary verbiage, as "/" by itself means "and/or"). Applicants' representative would like to thank Examiner Koyama for her courtesy in conducting the interview and for her assistance in resolving issues.

Claims 1 and 13 are the sole rejected independent claims and stand rejected under 35 U.S.C. § 103 as being unpatentable over Asami '100 ("Asami") in view of Dreifus '621 ("Dreifus") and Kakiage et al. '166 ("Kakiage"). This rejection is respectfully traversed for at least the following reasons.

Claim 1 recites in pertinent part, "state control means for halting the write and read processing on said buffer memory and said nonvolatile memory of said CPU ***while*** said transmission circuit is sending/receiving data to/from the outside" (emphasis added; claim 13 is

submitted to be patentable for at least reasons similar to those that will be discussed below with respect to claim 1).

Turning to the cited prior art, the Examiner admits that Asami in view of Dreifus fails to disclose or suggest the aforementioned feature. The Examiner therefore relies on Kakiage in an attempt to overcome the deficiencies of Asami in view of Dreifus. However, it is respectfully submitted that Kakiage is completely unrelated to the present invention; and any teachings from Kakiage used to modify Asami in view of Dreifus, even assuming *arguendo* proper, would not result in the claimed invention. Kakiage merely discloses a control circuit 4 which, as would be expected, stops the CPU 120 from reading from the read buffer until the data read from the external memory 150 is written into the read buffer data register. This is a conventional halting operation which prevents a reading operation where there is nothing to be read.

However, Kakiage is completely unrelated to an IC card and the functionality thereof in relation to the ***timing*** of the halt operation relative to the operations of a transmission circuit. Indeed, Kakiage is silent as to a corresponding "transmission circuit" relative to the alleged transmission circuit of Asami. Accordingly, even assuming *arguendo* proper, the proposed combination would not disclose or suggest "halting the write and read processing on said buffer memory and said nonvolatile memory of said CPU ***while said transmission circuit is sending/receiving data to/from the outside***." Instead, the proposed combination would, at best, result in the conventional halting of CPU read operations when there is no data to be read, ***independent of the transmission circuit operation***. In contrast, one of the features of the present invention is related to not only the halt operation itself, but the timing of the halt operation in relation to the transmission circuit of an IC card. As discussed above, Kakiage does not disclose

an IC card with a transmission circuit, let alone suggest performing the halt operation while a transmission circuit is sending/receiving data to/from the outside.

According to one aspect of the present invention, because the halt operation is performed while the transmission circuit is sending/receiving data to/from the outside, the influence of noise on the transmission circuit caused by the operations of the nonvolatile memory and the CPU can be suppressed. As a result, the reliability in send/receive processing by the transmission circuit can be improved (*see, e.g.,* page 3, line 23 – page 4, line 4 of Applicants' specification).

In view of the foregoing, it is respectfully submitted that neither Asami, Dreifus, nor Kakiage, alone or in combination, disclose or suggest "halting the write and read processing on said buffer memory and said nonvolatile memory of said CPU while said transmission circuit is sending/receiving data to/from the outside" as recited in claim 1 (similarly in claim 13). The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 1 and 13 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In

addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

For example, claim 9 recites "wherein said state control means operates to halt said nonvolatile memory while said transmission circuit is sending/receiving data to/from the outside." Kakiage does not halt the external memory 150 while the reading operation of the CPU is halted. In fact, the external memory 150 of Kakiage must operate while the CPU is halted from reading data from the read buffer. Indeed, if both the external memory 150 and the CPU are in a halt state, the data to be read would never be written into the read buffer from the external memory so that the data is never prepared in the read buffer and the CPU would never read data from the read buffer.

Based on the foregoing, it is submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

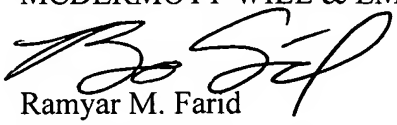
Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY, LLP.



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